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AN IMAGE SENSOR WITH TRANSPARENT TRANSISTOR GATES

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AN IMAGE SENSOR WITH TRANSPARENT TRANSISTOR GATES

FIELD OF THE INVENTION

The present invention relates to output circuits for image sensors and, more particularly, to such output circuits having a transparent conductor for a gate electrode gate.

BACKGROUND OF THE INVENTION

Charge coupled device (CCD) image sensors typically transfer electrons photogenerated in individual picture elements (pixels) to a charge detection circuit which is constructed on the same silicon substrate as the CCD. Prior art devices utilize polycrystalline silicon (polysilicon) gates in arrays of pixels. Prior art devices also include a so-called floating diffusion (FD) node whose voltage changes in response to electrons transferred to it by the shift registers which are part of the CCD. In order to detect the FD voltage changes, and transmit them to other circuits, one or more field effect transistors (FET's) are used to amplify, or buffer, and transmit the FD voltage changes to other circuits. Typically these FET's are also constructed with polysilicon gate electrodes. Polysilicon has been the preferred gate material for the FET gates due to its convenience, being also used as part of the CCD itself, and due to the proven reliability and the low electrical noise characteristics of the transistors with such gates.

Recently, however, CCD's have been developed where all the CCD gates are composed of transparent conducting oxide, such as indium-tin oxide (ITO). The amplifier transistors might, however, still be composed of polysilicon. Although output circuits made with polysilicon gates provide satisfactory electrical performance, they include drawbacks. One such drawback is that their inclusion with a CCD with all ITO gates, necessitates additional manufacturing complexity. It has been found, however, that FET's made with ITO gates also perform satisfactorily in output amplifier circuits. It is therefore an object of the present invention to provide output circuits made with transistor gates of transparent conducting oxide, such as indium tin oxide.

SUMMARY OF THE INVENTION

The present invention is directed to overcoming one or more of the problems set forth above. Briefly summarized, according to one aspect of the present invention, the invention resides in an image sensor having an image sensing portion for receiving incident light that is converted to a plurality of charge packets; a transfer mechanism for transferring the charge packets from the image sensing portion; and an output structure that receives the charge packets from the transfer mechanism for transporting output signals from the image sensor, wherein the output structure comprises a transparent conductor for a gate electrode gate.

These and other aspects, objects, features and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of the basic elements of an image sensor in accordance with the present invention;

Fig. 2 shows in schematic form the output circuit 18 shown in Fig. 1;

Fig. 3 is a top view showing the layout of portions of the output circuit 18; and

Fig. 4 is a sectional view taken along lines 4-4 of Fig. 3.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Turning first to FIG. 1, there is shown in block diagrammatic form a full-frame image sensor 10. The image sensor 10 includes photo-elements 12 which collect charge as a linear function of the intensity of incident light and integration time, and as a non-linear function of incident light wavelength. Each photo-element represents one pixel of an image scene. These photo-elements can for example be photo-capacitors which accumulate electrons in an n region of a

buried channel. During readout, charge is transferred vertically from photo-capacitor to photo-capacitor in each column to a buried-channel horizontal charge-coupled device (CCD) 14. Each packet of electrons from each photo-element is sequentially delivered to a horizontal CCD element preceding an output gate 16 and then from this element through the output gate to an output circuit 18. The output circuit 18 is integrated on the same chip as the sensor 10. The output circuit 18 provides an output voltage V_{out} proportional to each packet of electrons (charge) it receives.

Turning now to FIG. 2, the output circuit 18 is shown in schematic form. In response to the removal of the pulse φR applied to the gate electrode 20 of a reset transistor Q_R, the transistor Q_R is turned off and shortly thereafter, charge is transferred from under the output gate 16 to a floating diffusion FD, 33. As shown in FIG. 4, the floating diffusion is actually the source electrode 33 of the transistor Q_R. When the pulse φR is applied, the transistor Q_R is turned on and the potential across the floating diffusion FD is returned to a reference level set by V_{RD}, the reset drain potential. When transistor Q_R is off, a potential well is created in the floating diffusion. Electrons are once again transferred to this potential well from the output gate 16. The floating diffusion 33 is electrically connected to the gate electrode of a transistor QD_1 of the first stage of the source-follower output amplifier 18. In this first stage, there are two transistors QD_1 and QL_1. Both these transistors continuously operate in a saturated mode. At the electrical junction of the transistors QD_1 and QL_1, a voltage is produced which follows the voltage level across the floating diffusion FD. This voltage is applied as an input to the gate electrode of transistor QD_2. The drain of QD_2 is connected to the same potential source V_{DD} which is coupled to the drain of transistor QD_1. All of the transistors, Q_R, QD_1, QL_1 and QD_2 are NMOS lightly-diffused drain (LDD) buried-channel transistors. The source and drain electrodes are heavily-doped n^+, the channel region is under the gate electrode. Lightly-doped (n^-) source and drain (LDD and LDS) respectively connect the source and drain electrodes to the channel. The gate doesn't overlie the LDD and LDS regions. The output voltage V_{out} is taken from the source electrode of transistor QD_2. V_{out} is applied as an input to conventional off-chip signal processing circuitry.

FIG. 3 shows a top layout view of transistor Q_R and transistor QD_1 of the first stage of the source-follower output amplifier 18. FIG. 3 should be consulted during the description of FIG. 4. Turning now to FIG. 4 where there is shown in cross-section the reset transistor Q_R and the output gate 16 and two gates of the horizontal CCD 14. The CCD 14 is shown as a two-phase device. There are two levels of polysilicon, poly-1 and poly-2 which respectively provide shift register gate electrodes 22 and 24. A substrate 26 is of a p-type conductivity and an n-type layer 28, which can be provided by implanting arsenic into the substrate 26, provides a buried-channel structure. Directly over the n-type layer 28 is a layer of thermally grown silicon dioxide 29. Directly over the p-type substrate 26 is a p^+ field threshold adjust implant 46 in the non-active regions of the device. Over the p^+ field threshold adjusted regions 46 is a thick field silicon dioxide layer 31 provided by a conventional LOCOS (Local Oxidation of Silicon) process.

CCD shift register electrodes 22 and 24 are formed on the thin gate oxide 29. Separating each of the electrodes is an insulating layer 30 of silicon dioxide which is provided by a conventional LTO (Low Temperature Oxide). The output gate 16 has a positive potential V_{OG} continuously applied to the electrode. If we assume that electrons are held under the last gate 24 of the horizontal shift CCD 14 and that at this time the gate potential φ_2 is reduced while the gate potential φ_1 is raised, the electrons will flow down a "potential hill" under the output gate 16 to the floating diffusion 33. At this time, the transistor Q_R is off; that is, signal electrons collect on the source electrode 33. The transistor Q_R is an NMOS LDD buried-channel transistor. The source electrode 33 provides the function of a floating diffusion FD. The electrode 33 is a floating diffusion because the potential developed across it is allowed to float when the transistor Q_R is off. The floating diffusion is provided at the PN junction between the n^+ diffused electrode and p (substrate) regions. Then when the pulse φR is applied to the gate electrode 20 of transistor Q_R, the transistor Q_R turns on and the potential across the floating diffusion 33 is reset by the electrons draining off onto the drain of transistor Q_R which is at a potential V_RD. During these times, a voltage change is produced across the floating diffusion which is electrically connected to the gate electrode 40 of transistor QD_1. It is instructive to note that the gate electrode 40 is

composed or made of indium tin oxide. Although only gate electrode 40 is shown as indium tin oxide, similar gate electrodes made also be made of indium tin oxide.

The invention has been described with reference to a preferred embodiment. However, it will be appreciated that variations and modifications can be effected by a person of ordinary skill in the art without departing from the scope of the invention.

PARTS LIST

10	full-frame image sensor
12	photo-element
14	buried-channel horizontal charge-coupled device (CCD)
16	output gate
18	output circuit/source-follower output amplifier
20	gate electrode
22	shift register gate electrode
24	shift register gate electrode
26	substrate
28	n-type layer
29	layer of thermally grown silicon dioxide
30	insulating layer of silicon dioxide
31	thick field silicon dioxide layer (LOCOS)
33	floating diffusion/source electrode
40	gate electrode
46	p^+ field threshold adjust implant